



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/098,550	03/18/2002	Lin-Hung Chen	MR3003-13	4945
4586	7590	07/12/2004	EXAMINER	
ROSENBERG, KLEIN & LEE 3458 ELLICOTT CENTER DRIVE-SUITE 101 ELLICOTT CITY, MD 21043			HUYNH, KIM T	
			ART UNIT	PAPER NUMBER
			2112	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/098,550

Applicant(s)

CHEN, LIN-HUNG

Examiner

Kim T. Huynh

Art Unit

2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 March 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-5, are rejected under 35 U.S.C. 102(e) as being anticipated by Watts, JR. et al. (Pub. No. US20020103005)

As per claim 1, Watts discloses a circuit system for data transmission between LPC devices, comprising:

- A first LPC bus (fig.3, 345,350) connected to a first LPC device; (fig.3, 300)
- A second LPC bus (fig.3, 355) connected to a second LPC device; (fig.3, 305) and
- A LPC host controller (fig.3, 325), able to drive said first LPC device through said first LPC bus and said second LPC device through said second LPC bus. [0026]

As per claim 3, Watts discloses wherein said first LPC device is a master LPC device. [0026], (fig.3, 300)

Art Unit: 2112

As per claim 4, Watts discloses wherein said second LPC device is a slave LPC device. [0026], (fig.3, 305)

As per claim 5, Watts discloses wherein said first LPC bus and said second LPC bus are connected to a plurality of LPC devices, respectively. [0026]

3. Claims 6-10, 13-19, are rejected under 35 U.S.C. 102(e) as being anticipated by Shaw (US Patent 6,732,216)

As per claim 6, Shaw discloses a method for data transmission between LPC devices, comprising the steps of:

- Starting a first cycle through a first LPC bus by an LPC host controller, wherein a first LPC device sends a request to have a transaction with a second LPC device, and inserting a plurality of wait states after said request is received by said LPC host controller; and (col.4, lines 26-56), (col.5, lines 12-24), wherein set of registers (transactions) pending implies transactions in wait states)
- Starting a second cycle through a second LPC bus(fig.2, 125) by said LPC host controller, wherein said LPC host controller has a transaction with said second LPC device according to said request from said first LPC device. (col.4, lines 26-56)

As per claim 7, Shaw discloses wherein said request is a request for reading data from said second LPC device. (col.5, lines 12-24)

As per claim 8, Shaw further comprising the steps of:

- Stopping inserting said first LPC bus with wait states after said cycle on said second LPC bus is terminated; and (col.5, line 46-col.6, line 15)
- Terminating said cycle on said first LPC bus after said LPC host controller responds said first LPC device with said data from said second LPC device. (col.5, line 46-col.6, line 15)

As per claim 9, Shaw discloses wherein said request is a request for writing data into said second LPC device. (col.5, lines 12-24)

As per claim 10, Shaw discloses the method further comprising the steps of:

- Stopping inserting said first LPC bus with wait states after said cycle on said second LPC bus is terminated; and (col.5, line 46-col.6, line 15)
- Terminating said cycle on said first LPC bus. (col.5, line 46-col.6, line 15)

As per claim 12, Shaw discloses wherein each of said slave LPC devices further comprises an address register. (col.1, lines 35-47)

As per claim 13. Shaw discloses a method for data transmission between LPC devices, comprising the steps of:

- starting a first cycle through an LPC bus by an LPC host controller, wherein said LPC host controller has a transaction with a master LPC device; (col.4, lines 26-56), (col.5, lines 12-24)

Art Unit: 2112

- transmitting a request signal from said master LPC device through said LPC bus to said LPC host controller for having a transaction with at least one slave LPC devices; and (col.5, lines 12-24)
- starting a second cycle through said LPC bus by said LPC host controller, wherein said LPC host controller has a transaction with said slave LPC devices according to said request from said master LPC device. (col.4, lines 26-56)

As per claim 14, Shaw discloses wherein said request is a request for reading data from said slave LPC devices. (col.5, lines 12-24)

As per claim 15. Shaw discloses the method further comprising the steps of:

- recording the address of said data in an address register installed in said master LPC device so as to identify said data; and (col.5, lines 25-45)
- responding an arbitrary data value after said LPC host controller has received said reading request from said master LPC device. (col.5, line 46-col.6, line 15)

As per claim 16, Shaw discloses the method further comprising a step of: recording said address of said data in an address register installed in said LPC host controller after said LPC host controller has received said reading request from said master LPC device so as to identify said data. (col.5, lines 13-45)

Art Unit: 2112

As per claim 17. Shaw discloses the method further comprising the steps of:

- responding said reading request from said LPC host controller and transmitting said data from said slave LPC devices to said LPC host controller; and (col.5, lines 13-45)
- monitoring said data transmitted from said slave LPC device through said LPC bus, then said master LPC device can identify and obtain said data recording to said address recorded in said address register installed in said master LPC device. (col.5, line 13- col.6, line 15)

As per claim 18. Shaw discloses wherein said request is a request for writing data into said slave LPC device. (col.5, lines 12-21)

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watts, JR. et al. (Pub. No. US20020103005) in view of Shaw (US Patent 6,732,216)

6. As per claim 2, Watts discloses all the limitations as above except wherein said LPC host controller further comprises an address register.

Art Unit: 2112

However, Shaw discloses typically compuer architectures provide for one set of registers with each register assigned to a particular peripheral or i/o device. The information contain in the registers provide addresses and access content to the CPUs. (col.1, lines 1-47)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Shaw's teaching into Watt's system so as to provide maximum processing capability for the multiple systems in the computer architecture, allow continuous processing and computing and avoid the need to reset or place in a suspend state any or all the processors. (col.3, lines 15-23)

7. As per claims 11-12, Watts discloses a circuit system for data transmission between LPC devices, comprising:

- A LPC bus; (fig.3, 345)
- A master LPC device (fig.3, 300) connected to said LPC bus,
- At least one slave LPC devices (fig.3, 305) connected to the LPC bus; (fig.3, 355) and
- A LPC host controller, able to drive said master LPC device and said slave LPC devices through said LPC bus; [0026]

Watts discloses all the limitations as above except wherein said LPC host controller and said master/slave LPC device comprises an address register. However, Shaw discloses typically compuer architectures provide for one set of registers with each register assigned to a particular peripheral or i/o device. The information contain in the

Art Unit: 2112

registers provide addresses and access content to the CPUs. (col.1, lines 1-47)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Shaw's teaching into Watt's system so as to provide maximum processing capability for the multiple systems in the computer architecture, allow continuous processing and computing and avoid the need to reset or place in a suspend state any or all the processors. (col.3, lines 15-23)

Conclusion

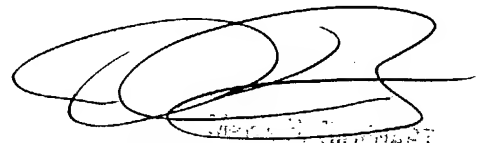
8. *Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM-6:30PM.*

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

June 16, 2004



MARK RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100